Abstract

A ferroelectric memory device features a main cell array, a row redundancy cell array, a first column redundancy cell array, a second column redundancy cell array, a main bitline pull-up controller, and a column selection controller. The main cell array includes a bitline structure comprising a main bitline and a sub bitline. The row redundancy cell array is configured to share the main bitlines with the main cell array. The first column redundancy cell array is configured to share wordlines and platelines with the main cell array. The second column redundancy cell array is configured to share redundancy wordlines and redundancy platelines with the row redundancy cell array, and to share redundancy main bitlines with the first column redundancy. The main bitline pull-up controller pulls up main bitlines and the redundancy main bitlines in response to first control signals, respectively. The column selection controller connects data bus lines to the main bitlines and the redundancy main bitlines in response to column selection signals, respectively.